CLAIMS

What is claimed is:

1. A system comprising:

a calculator that provides an indication of slack for at least one node of a circuit design, the at least one node being capable of operating transparently and non-transparently, the indication of slack being determined based on a minimum slack value for paths that include the at least one node, regardless of path transparency.

2. The system of claim 1, wherein at least one path that includes the at least one node is a non-transparent path based on timing information for the at least one path.

3. The system of claim 1, wherein the at least one node further comprises at least one latch.

4. The system of claim 1, wherein the at least one node further comprises a plurality of latches arranged to define at least one path, alternating latches along the at least one path being clocked by substantially out-of-phase clock signals to propagate a signal along the at least one path.

5. The system of claim 4, wherein the at least one path has a non-transparency based on timing information for the circuit design.

6. The system of claim 5, wherein the at least one path has at least one non-transparent latch based on the timing information.

7. The system of claim 1, further comprising a path tracer that traces each path that includes the at least one node, regardless of path transparency, the calculator determining slack for the paths traced by the path tracer.

8. The system of claim 7, wherein the path tracer traces through a downstream portion of at least one path that includes the at least one node, regardless of transparency of the at least one node.

9. The system of claim 7, further comprising a potential slack calculator that ascertains a minimum slack value associated with the at least one node according to a minimum of the slack determined for the paths traced by the path tracer.

10. The system of claim 7, wherein at least one path through the at least one node operates non-transparently based on timing information provided by timing analysis for at least a portion of the circuit design.

11. The system of claim 1, further comprising a timing analysis system that provides timing information associated with circuit components for paths that include the at least one node, the slack calculator determining the indication of slack for the at least one node based on the timing information.

12. A computer implemented design tool comprising the system of claim 1.

13. A system to facilitate design of an integrated circuit, comprising:

a path tracer that traces paths associated with a given node of a circuit design, regardless of path transparency; and

a calculator that determines timing characteristics associated with the given node based on timing information for the traced paths, a minimum timing characteristic being selected from the timing characteristics determined for the traced paths associated with the given node.

14. The system of claim 13, wherein the timing characteristic comprises slack and the timing constraint comprises a potential slack associated with the given node.

15. The system of claim 13, wherein the given node further comprises circuitry capable of operating transparently and non-transparently.

16. The system of claim 13, wherein at least one of the paths further comprises a plurality of latches arranged along the at least one of the paths, the plurality of latches being clocked by substantially out-of-phase clock signals to propagate a signal along the at least one of the paths.

17. The system of claim 13, wherein the at least one of the paths has a non-transparency according to corresponding timing information for the circuit design.

18. The system of claim 13, further comprising a potential slack calculator that determines the timing characteristic as a minimum slack value that is associated with the given node, the potential slack calculator determining the minimum slack value based on timing information for the traced paths according to a minimum of slack determined for each of the paths traced by the path tracer.

19. The system of claim 18, wherein at least one of the paths traced through the given node operates non-transparently based on the timing information.

20. The system of claim 13, further comprising a timing analysis system that provides the timing information associated with circuit components for the traced paths.

20. A system comprising:

means for tracing at least one path that includes a given node of a circuit design by analyzing the at least one path transparently, the given node being capable of operating transparently and non-transparently; and

means for determining potential slack for the given node, the potential slack corresponding to a minimum slack value determined from slack values associated with the given node, including a slack value associated with the at least one path, based on timing information for the at least one path.

21. The system of claim 20, further comprising means for determining slack for each of the paths traced by the means for tracing, the potential slack corresponding to minimum of the slack determined for paths traced by the means for tracing.

22. The system of claim 20, wherein the means for tracing is operative to trace each path associated with the given node regardless of path transparency.

23. The system of claim 22, further comprising means for determining slack for each of the paths traced by the means for tracing, the potential slack corresponding to minimum slack value from the slack determined for each of the paths traced by the means for tracing.

24. The system of claim 20, wherein the at least one of the paths further comprises plural means for latching an input signal from an input port to an output port based on a clock signal, the plural means for latching arranged along the at least one path such that adjacent pairs of the means for latching are activated to propagate a signal therethrough with substantially out-of-phase clock signals.

25. The system of claim 20, further comprising means for performing timing analysis on a circuit design that includes the at least one path to provide the timing information associated with circuit components for the at least one path.

26. A computer-readable medium having computer-executable instructions for performing a method comprising:

computing slack associated with a given node of a circuit design by analyzing each path associated with the given node transparently; and

determining a potential slack value as a minimum of the computed slack associated with the given node.

27. The computer-readable medium of claim 26, wherein the computing further comprises employing timing analysis information for the circuit design to compute the slack associated with the given node for each path associated with the given node.

28. The computer-readable medium of claim 26, wherein the given node is capable of operating transparently and non-transparently based on a control signal.

29. The computer-readable medium of claim 26, wherein at least one path associated with the given node comprises a plurality of latches arranged along the at least one path and being clocked by substantially out-of-phase clock signals for propagating a signal along the at least one path.

30. The computer-readable medium of claim 26, further comprising computer-executable instructions for tracing at least one path associated with the given node to enable a corresponding slack computation for the at least one path regardless of path transparency.

31. A method comprising:

determining a timing characteristic for a first path associated with a node of a given circuit design;

determining the timing characteristic for at least a second path, regardless of path transparency, the second path including the node and at least a portion of the second path being capable of operating transparently and non-transparently; and

providing an indication of timing performance associated with the node according to a minimum of the timing characteristic for a first path and the timing characteristic for at least a second downstream path.

32. The method of claim 31, wherein at least one of the first and second paths is a non-transparent path based on timing information associated with the circuit design.

33. The method of claim 31, wherein the timing characteristic is at least one of slack and clock skew associated with the node.

34. The method of claim 31, further comprising employing timing information obtained for the circuit design to compute each timing characteristic as a respective slack value associated with the given node for each path associated with the node.

35. The method of claim 34, further comprising tracing each path associated with the node transparently to enable a corresponding slack computation for each path associated with the node regardless of path transparency.

36. The method of claim 31, wherein the node comprises circuitry capable of operating transparently and non-transparently.

37. The method of claim 31, wherein at least one of the first and second paths associated with the node comprises a plurality of latches arranged along the respective

path in which each adjacent pair of the plurality of latches along the respective path are clocked by substantially out-of-phase clock signals for propagating a signal along the respective path.

38. A computer-readable medium having computer-executable instructions for performing the method of claim 31.